

#### REMARKS

Claims remaining in the present patent application are numbered 1-29. No amendments have been made. The rejections and comments of the Examiner set forth in the Office Action dated November 26, 2004 have been carefully considered by the Applicants. Applicants respectfully request the Examiner to consider and allow the remaining claims.

#### §112 Rejection

The present Office Action rejected Claims 1-29 under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. More particularly, the present Office Action objected to the claim limitation "a fixed pixel border having a predetermined width," as recited in Claims 1-3, 10, 13, 14, 19, and 20, and "a fixed dimension of n rows and m columns," recited in Claim 25.

For independent Claims 1, 13, and 19, Applicants respectfully assert that there is sufficient support for a "fixed" pixel border, and a pixel border of "fixed" dimension. Applicants hereby reassert and incorporate the

§112 arguments set forth in their reply to the Office Action dated November 26, 2004.

In summary, the specification describes a pixel border of width  $x$ . The width is not variable, but is predetermined to a specific value for  $x$ . In an example given,  $x$  is a predetermined value and can take a value between 1 and 5 pixels. That is, in one particular application of a pixel border in a display screen,  $x$  is predetermined to a value between 1 and 5, for example, 2 pixels in width.

Support for the "fixed" pixel border is found in the specification. In particular, Applicants respectfully point out that the specification recites that the "pixel border region 312 . . . [has] a predetermined pixel width,  $x$ ." (See lines 5-6, page 19). The predetermined pixel width,  $x$ , does not vary in one application (e.g., a manufactured display screen), but can vary in different applications (e.g., multiple display screens). That is, in one application of a pixel border in a display screen, the width,  $x$ , is fixed to 2 pixels. In another application of the pixel border in another display screen, the width,  $x$ , is fixed to 5 pixels.

Further, on page 21, lines 15-16, the specification in conjunction with Figure 9 provide a concrete example of a

pixel border having an unvarying width of two pixels. That is, as stated and shown in Figure 9, the width of the pixel border is fixed to two pixels, in one embodiment.

Specifically, as shown in Figure 9, the row drivers 450a-d and the column drivers 440a-d are configured to control the pixel border region 312. That is, the row and column drivers as shown in Figure 9 can only drive a pixel border having a width of two pixels. The row 450a-d and column drivers 440a-d are unable to drive additional pixels outside of the defined pixel border regions 312, that is fixed to two pixels in width. That is, no further control is shown for selecting between various rows and columns to vary the width of the pixel border region. As such, the embodiment of the present invention as shown in Figure 9 illustrates that the pixel border region 312 is fixed to 2 pixels in width. Figure 9, as well as accompanying text in the specification, provide support for other embodiments in which the pixel border region is fixed to 1, 3, 4, 5, etc. pixels in width, depending on the application.

Thus, Applicants respectfully submit that the specification sufficiently supports a "fixed" pixel border, and a pixel border of "fixed" dimension. As such, Claims 1-3, 10, 13, 14, 19, and 20 overcome the \$112 objections. Applicants respectfully request further examination of Claims 1-2, 10, 13, 14, and 19.

As to independent Claim 25, Applicant respectfully asserts that the frame buffer region is fixed, in one embodiment. As shown in Figures 7 and 9, and their accompanying text, the frame buffer region 314 is oriented in  $n$  rows and  $m$  columns ( $m \times n$ ). The frame buffer region 314 contains a "matrix of discrete pixels . . . according to a variety of display dimensions and formats." That is, the size of the frame buffer region 314 does not vary in one application (e.g., manufactured display screen), but can vary between different applications (e.g., multiple display screens). For example, the specification gives an example where the frame buffer region in one application of a frame buffer region in a display screen is of dimension, 160 pixels by 160 pixels. In another application of a frame buffer region in another display screen, the frame buffer region is of another dimension, e.g., 200 pixels by 200 pixels.

Thus, Applicants respectfully submit that the specification sufficiently supports a "fixed" frame buffer region. As such, Claim 25 overcomes the §112 objections. Applicants respectfully request further examination of Claim 25.

35 U.S.C. §103 Rejection

The present Office Action rejected Claims 1-5, 8, 13-16, 19-23, 25, 26, 28, and 29 under 35 U.S.C. 103(a) as being unpatentable over the Taniguchi reference (U.S. Patent No. 4,824,212) in view of Yokota et al. (U.S. Patent No. 6,181,313). Applicants have reviewed the above cited references and respectfully submit that the present invention as described in embodiments of independent Claims 1, 13, 19, and 25, is neither anticipated nor rendered obvious by the Taniguchi reference taken alone or in combination with the Yokota et al. reference.

Independent Claims 1, 13, 19, and 25

Applicants respectfully point out that the present invention as described in embodiments of independent Claims 1, 13, and 19 includes, in part:

a fixed pixel border having a predetermined width, said fixed pixel border surrounding said passive matrix and comprising a plurality of pixels each of which is uniformly controlled between an on and an off state as applied to each pixel by a common threshold signal . . .

(Emphasis Added)

Moreover, Applicants respectfully point out that the present invention as described in embodiments of independent Claim 25 includes, in part:

a pixel border surrounding said passive matrix and comprising a plurality of pixels each of which is uniformly controlled between an on and an off state as applied to each pixel by a common threshold signal.

(Emphasis Added)

Embodiments of the present invention as recited in independent Claims 1, 13, 19, and 25 pertain to a controllable pixel border for a negative mode passive matrix display device. In particular, the present invention as described in embodiments of independent Claims 1, 13, 19, and 25 recites that a pixel border, or fixed pixel border, that surrounds the passive matrix is uniformly controlled as applied to each pixel in the pixel border by a common threshold signal.

Applicants respectfully agree that it is conceded that the Taniguchi reference does not teach the limitations of a plurality of pixels which is uniformly controlled between an on and an off state by a common threshold signal, as is recited in independent Claims 1, 13, 19, and 25 of the present invention.

Moreover, Applicants respectfully note that the prior art reference, Yokota et al. fails to overcome the shortcomings of the Taniguchi reference. That is, the Yokota et al. reference also fails to teach or suggest the present display unit that comprises, in particular, the pixel border that surrounds a passive matrix, and where each of the pixels in the pixel border is uniformly controlled between an on and off state as applied to each

pixel by a common threshold signal, as claimed in independent Claims 1, 13, 19, and 25 of the present invention. Applicants hereby reassert and incorporate the \$103 arguments set forth in their reply to the Office Action dated November 26, 2004, and provide further arguments below.

Additionally, in contrast to independent Claims 1, 13, 19, and 25 of the present invention, the Yokota et al. reference, discloses a liquid display controller that can select part of the rows of a liquid crystal panel for display, such that the display is selectively produced on a portion of the liquid crystal display panel at a low voltage with a low-duty drive. That is, all of the rows in the Yokota et al. reference are capable of generating an image for display, and none are specifically assigned to be a pixel border. As such, the Yokota et al. reference teaches a variably sized pixel border. That is, the Yokota reference does not disclose a pixel border, but a display region that can partially select rows in the display to not display images in a variably sized pixel border region, which is distinct from embodiments of the present invention.

In addition, Applicants respectfully disagree that with regards to Figures 14K and 14L the Yokota et al. reference teaches a pixel border that is uniformly

controlled by a common threshold signal applied to each pixel, as recited in independent Claims 1, 13, 19, and 25 of the present invention. In particular, for references purposes, the relevant section of the Yokota et al. reference is repeated below, as follows:

In the first frame (frame I), the selection level of the common signal COM 2 is V1 and the non-selection level is V5. In the first frame (frame 1), the selection level of the segment signal SEG2 is GND and the non-selection level is V4. Any dot turns on when the voltage obtained by subtracting the potential of the segment signal from the potential of the common signal, exceeds the threshold value of the liquid crystal. The difference in the potential is used as a pixel signal D. Therefore, the dot at the intersecting point of the transparent electrode ECOM2 and the transparent electrode ESEG2 is turned on. (See col. 14, lines 43-53)

In particular, Applicants respectfully assert that the Yokota et al. reference teaches that a dot, or pixel, is turned on when the voltage obtained by subtracting a segment signal from the common signal exceeds a threshold level of the liquid crystal. That is, generally any dot in the display matrix will turn on when the voltage applied to that dot exceeds a threshold level.

Specifically, the Yokota et al. reference does not teach or disclose that dots corresponding to a pixel border are grouped together and uniformly controlled by a common control signal as applied to each pixel in the pixel



border. Instead, the Yokota et al. reference teaches that those dots in the pixel border are each separately controlled and are turned on when the difference voltage of the segment (column) and common signals for each of the rows exceeds the threshold value for each pixel. That is, Figures 14K and 14L illustrate that each of the dots (pixels) are separately controlled. As such, after the size of the pixel border is determined, each of those pixels belonging in the pixel border is controlled by a separately controlled signal, and not a common threshold signal as applied to each pixels in the border region, as is recited in independent Claims 1, 13, 19, and 25 of the present invention.

Moreover, Applicants respectfully assert that the use of the term "common signal" in the Yokota et al. reference is not analogous to the use of the term "common threshold signal," as recited in independent Claims 1, 13, 19, and 25. In particular, the use of the term "common signal" refers only to the signal applied to a particular row of dots or pixels, and is distinct from the common threshold voltage as recited in the present invention. That is, a "common signal" is applied to a particular row of pixels. Another "common signal" is applied to another row of pixels, and so on. For example, common signal COM 2 is applied to the second row of pixels in Figure 14L, and common signal COM 3 is applied to the third row of pixels

in Figure 14L. As such, the row common signals can have different values since the pixels in the Yokota et al. reference can both display images or display a border region. On the other hand, the common threshold voltage as recited in independent Claims 1, 13, 19, and 25 is uniformly applied to each of the pixels in the pixel border region.

In addition, Applicants respectfully assert that the use of the term "threshold level" in the Yokota et al. reference is not analogous to the use of the term "common threshold signal," as recited in independent Claims 1, 13, 19, and 25. The use of the term "threshold value" refers only to a threshold voltage above which a pixel will turn on and below which a pixel will turn off. The use of the term "threshold value" is distinct from the "common threshold signal" as recited in the present invention. The threshold value in the Yokota et al. reference is a reference value used for comparison, whereas on the other hand, the "common threshold signal" is uniformly applied to each of the pixels in the pixel border region, as is recited in independent Claims 1, 13, 19, and 25.

Specifically, the present invention, on the other hand, claims a display unit that has distinct display and border regions. In particular, the present invention also discloses a separate pixel border that surrounds the

passive matrix that is uniformly controlled between an on and off state by a common threshold signal, as recited in independent Claims 1, 13, 19, and 25 of the present invention.

Figure 9 of the present Application describes the application of the common threshold signal to control the pixels in the fixed pixel border. The common threshold signal is defined as the voltage difference between threshold voltage drivers 430a and 430b in their on or off states. In particular, the threshold voltage (V2) of the common threshold signal is commonly applied to each of the pixels of the fixed pixel border in the on state, and the threshold voltage (V1) of the common threshold signal is commonly applied to each of the pixels of the fixed pixel border in the off state.

Moreover, independent Claim 13 recites that each of the plurality of pixels is uniformly controlled between an on and an off state as applied to each pixel by a "common threshold signal" that is generated from a common row threshold voltage and a common column threshold voltage. That is, the threshold voltage drivers for the rows and columns generate the common row threshold voltages and the common column threshold voltage that are used to generate the common threshold signal, as applied to each of the pixels in the pixel border region. Neither the Taniguchi

et al. nor the Yokota et al. references teach the use of the common row and column threshold voltages to generate the common threshold signal that is applied to each of the pixels in the fixed border region.

Thus, Applicants respectfully submit that the present invention as disclosed in independent Claims 1, 13, 19, and 25 is not anticipated or rendered obvious by the Taniguchi taken alone or in combination with the Yokota et al. reference, and is in a condition for allowance. In addition, Applicants respectfully submit that Claims 2-12 which depend from independent Claim 1 are also in a condition for allowance as being dependent on an allowable base claim. Also, Applicants respectfully submit that Claims 14-18 which depend from independent Claim 13 are also in a condition for allowance as being dependent on an allowable base claim. Further, Applicants respectfully submit that Claims 20-24 which depend from independent Claim 19 are also in a condition for allowance as being dependent on an allowable base claim. Additionally, Applicants respectfully submit that Claims 26-29 which depend from independent Claim 25 are also in a condition for allowance as being dependent on an allowable base claim.

#### CONCLUSION

In light of the facts and arguments presented herein, Applicants respectfully request reconsideration of the rejected Claims.

Based on the arguments presented above, Applicants respectfully assert that Claims 1-29 overcome the rejections of record. Therefore, Applicants respectfully solicit allowance of these Claims.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

Wagner, Murabito & Hao LLP

Date:

20 September 2005

  
\_\_\_\_\_  
Lin C. Hsu

Reg. No.: 46,315

Two North Market Street

Third Floor

San Jose, California 95113